Single electron tunneling transistor with tunable barriers using silicon nanowire metal-oxide-semiconductor field-effect transistor

Akira Fujiwara,[a] Hiroshi Inokawa, Kenji Yamazaki, Hideo Namatsu, and Yasuo Takahashi[b]
NTT Basic Research Laboratories, NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan

Neil M. Zimmerman and Stuart B. Martin
National Institute of Standards and Technology (NIST), 100 Bureau Drive, Gaithersburg, Maryland 20899

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We have achieved the operation of single-electron tunneling (SET) transistors with gate-induced electrostatic barriers using silicon nanowire metal-oxide-semiconductor field-effect transistor (MOSFET) structures. The conductance of tunnel barriers is tunable by more than three orders of magnitude. By using the flexible control of the tunable barriers, the systematic evolution from a single charge island to double islands was clearly observed. We obtained excellent reproducibility in the gate capacitances: values on the order of 10 aF, with the variation smaller than 1 aF. This flexibility and controllability both demonstrate that the device is highly designable to build a variety of SET devices based on complementary metal-oxide-semiconductor technology. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2168496]

In past decades, single-electron tunneling (SET) devices[1] have been extensively studied for a wide range of applications such as low-power large-scale integration (LSI) circuits,[2,3] ultrasensitive electrometers,[4] and metrological standards.[5] While the conventional metal-based SET devices use fixed tunnel barriers made of metal oxide, the use of electrostatic potential barriers by gate electrodes has become possible in semiconductor devices, e.g., in GaAs-based SET devices.[6] These barriers are electrically tunable, giving us a chance to control the tunnel conductance over a wide range and thereby providing the degree of freedom to control coulomb blockade (CB) and/or the configuration of charge islands in a more flexible way.

Among semiconductor SET devices, silicon-based devices have been investigated mostly in the context of LSI application. In spite of the attempts to fabricate high-temperature operating devices with various techniques,[3] including the use of electrostatic barriers,[7,8] it is still hard to see sufficient controllability in device parameters such as capacitance and tunnel conductance. It is important to develop a standard way of fabricating devices reproducibly and find out the scaling rule, as is always sought in Si device technology.

We report here the operation of Si SET transistors with tunable barriers fabricated by standard Si metal-oxide-semiconductor field-effect transistor (MOSFET) technology. Each transistor consists of a Si nanowire channel and fine gates to form the electrostatic barriers. In our previous work[9] we found that our devices showed small but periodic CB oscillations of SET transistors at 20 K by means of a special voltage-sweep method. In this letter we demonstrate the highly reproducible operation below 4 K and the flexible design of the device due to the tunable electrostatic barriers.

Figure 1(a) shows the schematic top view and the cross-sectional view of the device. The ⟨110⟩-oriented Si-wire channel and lower poly-Si gates (LGS, LGC, LGD) are fabricated by electron beam lithography on a (001) silicon-on-insulator wafer. The wide upper poly-Si gate (UG) is used as an implantation mask during the formation of an *n*-type source and drain. The thicknesses and width of the Si wire, the gate SiO_2, and the buried SiO_2 are about 20, 20, 30, and 400 nm, respectively. The length of the lower gates is 10 nm. The UG intrudes into the 40-nm-long gap between lower gates. The thickness of the spacer SiO_2 between lower gates and UG is 30 nm. Figure 1(b) shows a top-view scanning electron microscope image of the device before the UG formation. The equivalent circuit diagram is depicted in Fig. 1(c). Three tunable barriers are controlled by the gate voltages to lower gates (V_{LGS}, V_{LGC}, V_{LGD}). The region sandwiched between the barriers acts as a charge island, which is mainly controlled by the upper gate voltage (V_{UG}), but also is

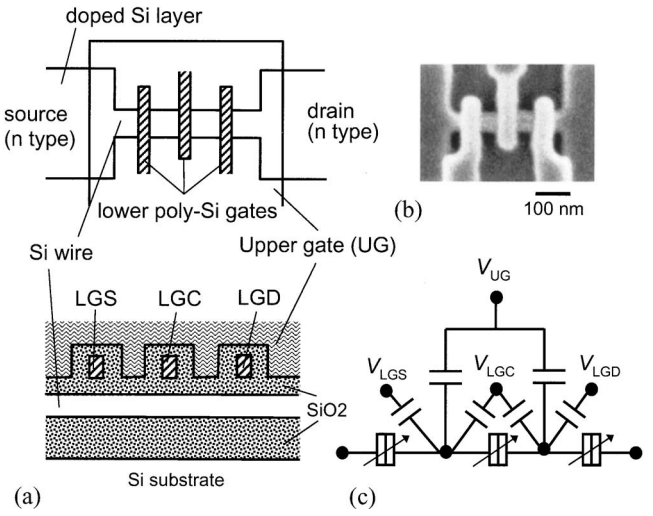

FIG. 1. (a) Schematic top view and cross-sectional view of the device. Three lower gates (LGS, LGC, LGD) are used to form tunnel barriers. (b) Top-view scanning electron microscope image of the device before the upper gate is formed. (c) Equivalent circuit of the device with tunnel barriers separately tuned by V_{LGS}, V_{LGC}, and V_{LGD}.

[a]Electronic mail: afuji@aecl.ntt.co.jp
[b]Present address: Graduate School of Information Science and Technology, Hokkaido University, Sapporo 060-0814, Japan.

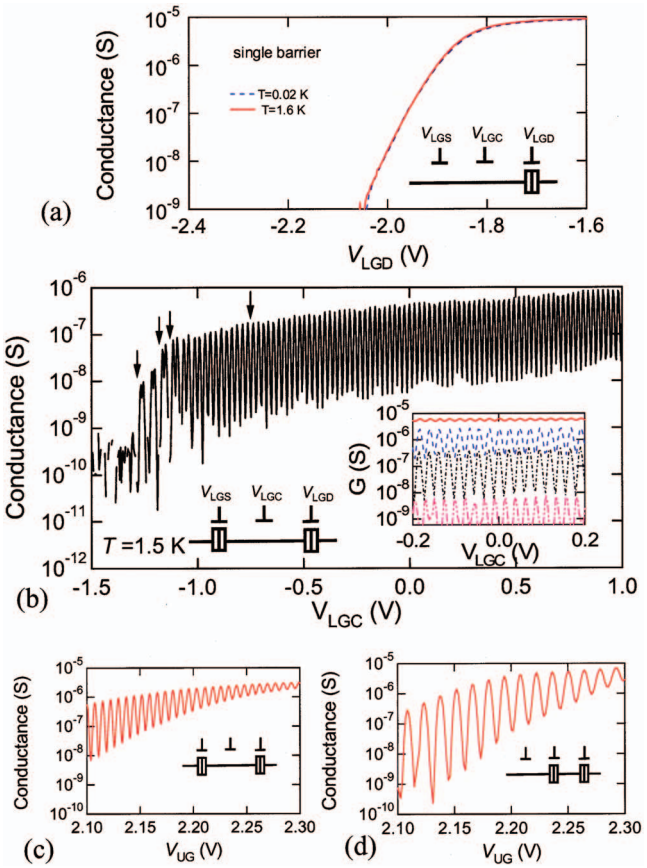

FIG. 2. (Color) Electrical characteristics (device 1). (a) Conductance of a MOSFET at LGD as a function of V_{LGD} at V_D=1 mV (the characteristics of the single barrier). (b) CB oscillation of the SET transistor consisting of the long island with two barriers (G=1 μS) at LGS and LGD (T=1.5 K, V_{LGS} =−2.352 V, V_{LGD}=−1.902 V, V_D=1 mV, and V_{UG}=2 V). The inset shows the results when G of each barrier is 8 μS, 4 μS, 1 μS, and 20 nS. (c) CB oscillation of the long island as a function of the upper gate voltage at V_{LGS}=−2.465 V, V_{LGC}=0 V, and V_{LGD}=−1.95 V. (d) CB oscillation of the short island with tunnel barriers at LGC and LGD (V_{LGS}=0 V, V_{LGC}= −1.426 V, and V_{LGD}=−1.95 V). The configurations of tunnel barriers are schematically shown in each figure.

coupled to lower gates via cross capacitances. Tunable barriers allow us to get various configurations of the charge islands: For example, a long island is formed if two barriers are formed under LGS and LGD while a short island is formed if LGC and LGD form barriers.

Conductance (G) characteristics of a single barrier formed under LGD are shown in Fig. 2(a). The source was grounded while the drain voltage (V_D) was 1 mV. V_{UG}, V_{LGS}, and V_{LGC} were fixed at 2, 0, and 0 V. In the subthreshold region when $V_{LGD}<-1.9$ V, the conductance showed exponential dependence on V_{LGD}, which seems to resemble thermally activated conduction of the conventional MOSFET. However, because the slope was almost independent of temperature up to 10 K, we attribute the dominant conduction below 10 K to the source-to-drain tunneling, as was reported previously using an 8-nm-gate MOSFET.[10] It was possible to vary the tunnel conductance by more than three orders of magnitude down to the noise floor of our measurement.

We now describe the operation of SET transistors using the electrostatic barrier. Figure 2(b) shows $G(V_{LGC})$ characteristics of a SET transistor when two barriers are formed under LGS and LGD. V_{LGD} and V_{LGD} are set so that the G of each barrier is equal to 1 μS when V_{LGC}=0 V. We obtained

TABLE I. The capacitances estimated from the CB oscillations for three identically patterned devices. The three possible configurations forming a single charge island are described: a long island (barriers formed by LGS and LGD), a short island (two barriers by LGS and LGC), and a short island (two barriers by LGC and LGD).

Capacitances	Device 1	Device 2	Device 3
	Long island / Short island (source side) / Short island (drain side) Units: (aF)		
C_{UG}	22/10/11	22/11/11	22/10/11
C_{LGS}	3.2/2.8/0.09	2.7/2.3/0.12	3.0/2.9/0.07
C_{LGC}	6.7/[a]/[a]	6.2/2.8/3.1	6.0/2.6/2.8
C_{LGD}	2.5/0.08/2.4	2.5/0.14/2.4	2.8/0.08/2.5

[a]Not measured.

a highly periodic CB oscillation in a broad range of V_{LGC}, except for the region below V_{LGC}=−1 V where application of V_{LGC} forms a third barrier under LGC to split a long island into two islands. In the periodic region where $V_{LGC}>-1$ V the deviation of the oscillation period was less than one percent.[11] The inset of Fig. 2(b) shows the $G(V_{LGC})$ curves for various conductances of the barrier. We were able to vary the peak conductance electrically by more than three orders of magnitude.

We used the different configurations of charge islands to estimate various gate capacitances (C_G). C_G was calculated by $e/\Delta V$ where ΔV is the period of the CB oscillation. For example, Fig. 2(c) shows the CB oscillations of the long island when UG was scanned, while Fig. 2(d) shows that of the short island formed between LGC and LGD. We can see that the upper gate capacitance (C_{UG}) of the short island was close to half that of the long island. A summary of the gate capacitances for three devices with an identical lithography design is in Table I. It is remarkable that the variation in C_{UG} (22 aF for the long island and 11 aF for the short one) was quite small, about 1 aF (about 10% of 11 aF) at most. The capacitances between the lower gates and islands (C_{LGS}, C_{LGC}, C_{LGD}) have also a variation smaller than 1 aF, although the relative variation gets larger.

The measured capacitances agree fairly well with calculated ones using a simplified geometry model. The capacitance of a cylindrical Si wire with a skin of SiO_2 is given by $C_G=2\pi\varepsilon L/\ln[(D_{OX}+D_{SI}/2)/(D_{SI}/2)]$; ε is the permittivity of SiO_2, L is the wire length, D_{OX} is the SiO_2 thickness, and D_{SI} is the wire diameter. For the short island, if we assume that UG is coupled to the wire part whose boundaries extend halfway under the spacer SiO_2 on both sides, the correspond-

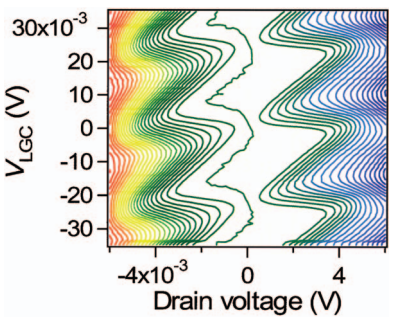

FIG. 3. (Color) The Coulomb diamonds in the contour plot of the drain current vs V_D and V_{LGC} (device 1, T=0.02 K, V_{UG}=2 V, V_{LGS}= −2.483 V, V_{LGD}=−1.957 V). Contour lines are 20 pA steps from low (red) to high (violet) in the range between −460 and 390 pA.

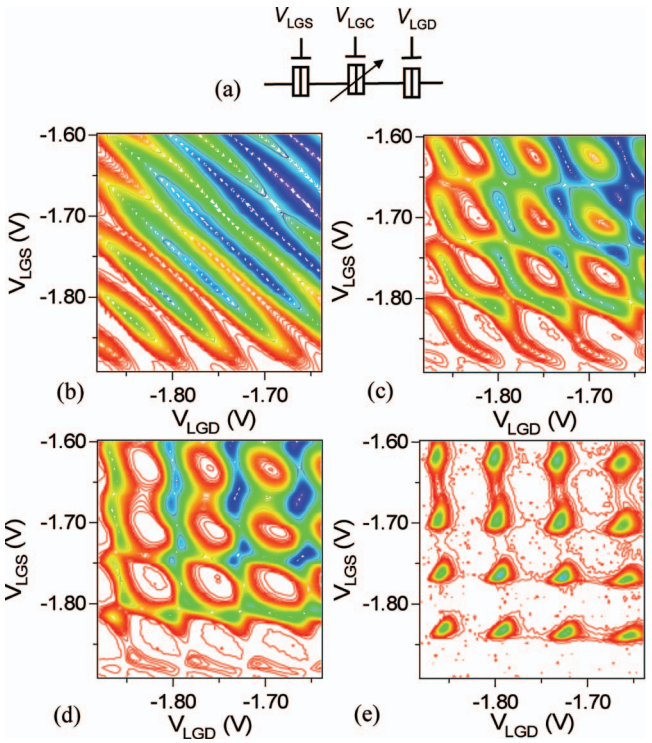

FIG. 4. (Color) Evolution from a single island to split double islands for device 2. (a) Equivalent circuit. (b)–(e), contour plots of the drain current vs V_{LGS} and V_{LGD} (T=0.02 K, V_D=1 mV, V_{UG}=2 V, V_{LGC}=−0.75, −1.13, −1.18, and −1.284 V, respectively). Each V_{LGC} is depicted by the arrow in Fig. 2(b). Contour lines run from low (red, 0 A) to high (violet, 1.4 nA) with 10-pA steps.

ing L is 70 nm. Then, C_{UG}11.0 aF when $\varepsilon=3.9\varepsilon_0$, D_{OX} =30 nm, and D_{SI}=20 nm. Similarly, for the longer island, C_{UG} and C_{LGC} are calculated to be 21.9 and 6.3 aF, respectively.

Figure 3 shows Coulomb diamond characteristics in the contour plot of the drain current versus V_{LGC} and V_D. The configuration was such that a long island was formed with tunnel barriers of conductance G=100 nS. From the shape of the diamond, we estimate the source and the drain capacitance to be about 6 aF for each. The total capacitance of the long island is therefore estimated to be 47 aF. The total capacitance of the short island with similar barriers is estimated to be about 30 aF.

Splitting of the charge island is demonstrated in Fig. 4. Figure 4(a) shows the equivalent circuit diagram. Figures 4(b)–4(e) show the contour plots of the drain current versus V_{LGS} and V_{LGD}. We changed V_{LGC} as a parameter to split a long island into double short islands. In Fig. 4(b) the central barrier is so low that the island is single; straight ridge lines corresponding to the peaks of CB oscillations run in parallel. As the barrier is raised in Figs. 4(c) and 4(d), the ridge lines are deformed into the so-called honeycomb lattice because the island is split into two coupled islands. In this transition where the coupling is tunable,[12] a larger current is obtained at the vertices of the lattice. The two islands become more isolated in Fig. 4(e) where the lattice is deformed into the parallelogram one. Large currents are obtained only at the vertices where the CBs at the two islands are lifted at the same time. The systematic evolution from the single island to double islands demonstrates that the control of the electrostatic barrier is effective in making and changing various configurations of charge islands.

We believe that the excellent controllability in these devices increases the potential of Si-based SET devices for a wider range of application. The category of the devices with tunable electrostatic potential, sometimes what we call a Si nanowire charge-coupled device (CCD),[13] is applicable to the metrological current standard. By taking advantage of dynamically varied barriers, we succeeded in the operation of a single-electron turnstile[14] and its application to multivalued memory.[15] Moreover, we are hopeful that we will be able to reduce the device size based on the scaling rule of MOSFETs; the devices presented here used the technology node between 45 and 65 nm that should be commercially available soon, around 2008.[16] We can expect that higher temperature operation will be achieved by the progressing complementary metal-oxide-semiconductor (CMOS) technology that will enter sub-10-nm minimum feature size.

In conclusion, we demonstrated the operation of SET transistors with electrostatic barriers using Si nanowire MOSFETs. Tunnel barriers were tunable in their conductance over three orders of magnitude, which enabled us to change the island configuration flexibly and observe systematic evolution from a single island to split double islands. The charge-island gate capacitances on the order of 10 aF showed excellent reproducibility with the deviation less than 1 aF.

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